Amendments to the Claims

The following Listing of Claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended): A method for creating a ~~sloped~~ via contact from a microelectronic device on a front side of a wafer to a back side of the wafer ~~having front and back sides~~, comprising:

~~providing a contact on the front side of the wafer;~~

forming ~~a sloped via in the wafer under the front contact~~ a via defined by sidewalls and extending through the wafer from a contact of the microelectronic device to the back side of the wafer, wherein the via has a width of at most 80 μm and at least a portion of the via has sloped sidewalls and a width that increases with distance through the wafer~~, the sloped via increasing in width~~;

coating the sidewalls ~~walls~~ of the ~~sloped~~ via with conductive material; and

~~providing a contact~~ forming on the back side of the wafer a back contact that is [[,]] electrically connected to the contact of the microelectronic device ~~front contact~~ through the conductive material coating the sidewalls of the ~~sloped~~ via.

Claim 2 (canceled)

Claim 3 (currently amended): The method of claim 1 [[2]], wherein the width of the via is at most ~~sloped via is no wider than~~ 50 um.

Claim 4 (currently amended): The method of claim 1 [[2]], wherein the coating of the sidewalls ~~walls~~ leaves a coating of conductive material ~~in the sloped via~~ at least 1000 Angstroms thick on the sidewalls where the via width is ~~the~~ narrowest.

Claim 5 (original): The method of claim 4, wherein the conductive material is selected from the group consisting of NiChrome and gold.

Claim 6 (currently amended): The method of claim 4, wherein the coating of the sidewalls ~~walls~~ includes plating.

Claim 7 (currently amended): The method of claim 1 [[2]], wherein the forming of the ~~a sloped~~ via comprises ~~includes~~:

forming in the wafer a preliminary via with a substantially constant width; and

widening at least a portion of the preliminary via to form the portion of the via having sloped sidewalls ~~so that its width increases from front to back~~.

Claim 8 (currently amended): The method of claim 7, wherein the forming of the [[a]] via comprises etching the wafer with ~~includes using~~ a deep reactive ion etching (DRIE) process.

Claim 9 (currently amended): The method of claim 8, wherein the forming of the [[a]] via comprises etching the wafer from only one of the front and back sides of the wafer ~~includes using a one-sided etch~~.

Claim 10 (currently amended): The method of claim 8, wherein the forming of the [[a]] via comprises etching the wafer from both the front and back sides of the wafer ~~includes using a two-sided etch~~.

Claim 11 (currently amended): The method of claim 7, wherein the widening of the via comprises etching the wafer with ~~includes using~~ an isotropic plasma etch.

Claims 12-22 (canceled)

Claim 23 (new): The method of claim 1, wherein the forming of the via comprises forming the portion of the via having sloped sidewalls with a width that increases from the contact of the microelectronic device to the back side of the wafer.

Claim 24 (new): The method of claim 1, wherein the portion of the via having sloped sidewalls extends from the contact of the microelectronic device to the back side of the wafer.

Claim 25 (new): The method of claim 1, wherein the via has a non-sloped portion.

Claim 26 (new): The method of claim 1, wherein the portion of the via having sloped sidewalls varies linearly with distance through the wafer.

Claim 27 (new): The method of claim 1, wherein the portion of the via having sloped sidewalls varies nonlinearly with distance through the wafer.